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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,170	12/04/2003	Raminda Udaya Madurawe		6747

33380 7590 09/14/2005

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EXAMINER	
LE, DON P	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 09/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/727,170	MADURAWE, RAMINDA UDAYA	
	Examiner	Art Unit	
	Don P. Le	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☒ Claim(s) *23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Madurawe (US 6,747,478)

The applied reference has a common inventor with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

3. With respect to claim 1, figures 1-17 of Madurawe disclose a programmable wire structure for an integrated circuit, comprising:

a programmable switch (transistor of figure 9) coupling two nodes (I1, O1), said switch having a first state that connects said two nodes, said switch having a second state that disconnects said two nodes; and

a configuration circuit (130, figure 3) coupled to said programmable switch, said circuit comprising a means to program said switch between said first and second state; and

a first metal layer (126, figure 3) fabricated above a silicon substrate layer, said switch and said configuration circuit fabricated substantially above said first metal layer.

4. With respect to claim 2, figure 3 of Madurawe discloses a second metal layer (140) is fabricated substantially above said switch and said configuration circuit.

5. With respect to claim 3, figure 9 of Madurawe discloses at least one of said first (I1) and second (O1) nodes is coupled to a node (30) in said first metal.

6. With respect to claim 4, figure 3 of Madurawe discloses the first metal and second metal layers are coupled to each other.

7. With respect to claim 5, Madurawe teaches thin film transistor (column 3, line 15).

8. With respect to claim 6, Madurawe discloses at least one of said first (39) and second (28) nodes of said programmable switch further comprises a via structure (column 5, line 1239), said via structure containing a seed metal, said seed metal facilitating a thermally activated phase change of at least one of said thin film materials to improve conduction of said connect state (metal connection as shown in figure 14A improves conduction).

9. With respect to claims 7 and 12, Madurawe teaches thin film transistors (see abstract).

10. With respect to claims 8, 9, 13, 14 and 22, Madurawe discloses a memory element is selected from one of fuse links, anti-fuse capacitors, SRAM cells, DRAM cells, metal optional links, EPROM cells, EEPROM cells, flash cells, ferro-electric elements, electrochemical elements, optical elements and magnetic elements (column 11, lines 65-70).

11. With respect to claims 10 and 16, figure 14 of Madurawe discloses a pass-gate device,

said pass-gate controlled by an output signal from said memory element (SRAM), said first state generated by an on pass-gate, and said second state generated by an off pass-gate; and a configuration access to program said memory data, said memory bit polarity generating an on and off control signal to select said state of pass-gate device.

12. With respect to claims 11 and 15, the programmable logic Madurawe teaches a wire structure for an integrated circuit having two selectable methods of connecting wires, comprising:

a first selectable method comprising programmable switches (figure 14), each said switch coupling a wire in a first set to a wire in a second set, and said method providing a means to program a user defined interconnect pattern between said first and second set of wires;

and a second selectable method comprising permanent connections in lieu of said switches, said permanent connection pattern duplicating one of said user defined interconnect patterns (ASIC section, column 5, lines 54-55).

13. With respect to claim 17, the apparatus of Madurawe has an array of programmable cells on a substrate layer.

14. With respect to claim 18, the apparatus of Madurawe discloses a semiconductor device for integrated circuits with two selectable manufacturing configurations, comprising:

a first module layer having an array of structured cells (122), said module layer having at least one layer of metal;

and a second module layer (126) formed substantially above said first module layer comprising two selectable configurations, wherein: in a first selectable configuration a programmable interconnect structure (figure 14) is formed to connect said structured cells, and in

a second selectable configuration a customized interconnect structure is formed to connect said structured cells.

15. With respect to claim 19, figure 3 of Madurawe discloses a third module layer (130) formed substantially above said second module layer comprised of a plurality of metal layers, said metal layers providing conductive wires to complete interconnect and routing of said semiconductor device.

16. With respect to claim 20, figure 4 of Madurawe discloses each said structured cell comprising inputs and outputs, said inputs and outputs formed in said first module layer; and a portion of said inputs and outputs requiring one of said selectable second modules to connect to each other.

17. With respect to claim 21, it is inherent in the apparatus of Madurawe (programmable logic device) said first selectable configuration comprised of a plurality of programmable interconnect patterns, a unique said pattern programmed by a user; and said second selectable configuration comprised of an interconnect pattern duplicating said unique programmed pattern; and said array of structured cells comprising an interconnect pattern, said interconnect pattern identical with either of said selectable options.

Allowable Subject Matter

18. Claim 23 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is an examiner's statement of reasons for allowance:

With respect to claim 23, the prior art does not teach fabricating hard wire controls to replicate a specific memory pattern, wherein replicating comprises: a logic zero memory output mapped to a hard wire disconnect; and a logic one memory output mapped to a hard wire connect.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Response to Arguments

20. Applicant's arguments with respect to claims 1-23 have been considered but are moot in view of the new ground(s) of rejection.

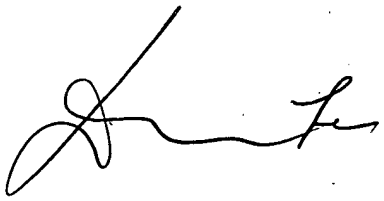
Conclusion

21. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Don P. Le whose telephone number is 571-272-1806. The examiner can normally be reached on 7AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael J. Tokar can be reached on 571-272-1812. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

9/12/2005



DON LE
PRIMARY EXAMINER